AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of processing pixel signals
~~levels~~, the method comprising:

clamping a pixel readout line to a voltage level less than a voltage
corresponding to a pixel signal;

subsequently coupling the pixel readout line to an output of <u>a source-</u>
<u>follower transistor</u> ~~an n-MOS source-follower~~ and reading out the pixel signal
onto the pixel readout line ~~through the n-MOS source-follower~~;

<u>clamping a capacitive storage node in a pixel signal processing circuit to a</u>
<u>voltage less than a voltage corresponding to the pixel signal appearing on the</u>
<u>pixel readout line;</u>

<u>subsequently coupling the pixel readout line to the storage node in the</u>
<u>processing circuit;</u> and

storing a signal corresponding to the pixel signal that was read out <u>on the</u>
<u>capacitive storage node</u>.

2. (Original) The method of claim 1 wherein clamping the pixel readout line
includes discharging a capacitance on the pixel readout line.

3. (Withdrawn) The method of claim 2 wherein discharging the pixel readout
line is performed while processing a previously-stored pixel signal.

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4. (Currently Amended) The method of claim 2 wherein <u>the</u> discharging the <u>capacitance on the</u> pixel readout line includes disabling a pixel selection switch.

5. (Currently Amended) The method of claim 2 wherein <u>the</u> discharging the <u>capacitance on the</u> pixel readout line includes enabling a switch to couple the pixel readout line to ground.

6. (Canceled)

8. (Currently Amended) The method of claim [[6]]<u>1</u> wherein the storage node is clamped to substantially the same voltage and at about the same time as the pixel readout line.

9. (Currently Amended) The method of claim [[6]]1 including:

resetting the pixel;

subsequently reading out a reset signal through the n-MOS source-follower; and

storing on a second capacitive storage node in the processing circuit a signal that corresponds to the reset signal.

10. (Original) The method of claim 9 including:

prior to storing the signal corresponding to the reset signal, clamping the second capacitive storage node to a voltage less than the voltage corresponding to the reset signal; and

subsequently coupling the pixel readout line to the second storage node to store the signal corresponding to the reset signal on the second storage node.

11. (Withdrawn) The method of claim 1 including passing the pixel signal that was read out through a p-MOS source-follower.

12. (Withdrawn) The method of claim 11 including:

clamping a capacitive storage node in a pixel signal processing circuit to a voltage greater than the pixel signal appearing at an input to the p-MOS source-follower, wherein the storage node is clamped before passing the pixel signal through the p-MOS source-follower to the processing circuit; and

subsequently coupling an output of the p-MOS source-follower to the storage node in the processing circuit.

13. (Withdrawn) The method of claim 12 including:

resetting the pixel after storing the signal corresponding to the pixel signal in the processing circuit;

subsequently reading out a reset signal through the n-MOS source-follower;

passing the reset signal through the p-MOS source-follower to the processing circuit; and

storing a signal corresponding to the reset signal in the processing circuit.

14. (Withdrawn) The method of claim 13 wherein, prior to passing the reset signal through the p-MOS source-follower, a second capacitive storage node in the processing circuit is clamped to a voltage level higher than the reset signal appearing at the input to the p-MOS source-follower.

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15. (Withdrawn) The method of claim 13 including converting a difference between the pixel and reset signals stored by the processing circuit to a corresponding set of digital signals.

16. (Currently Amended) An imager comprising:

a pixel readout line;

an active pixel sensor including a ~~an n-MOS~~ source-follower <u>transistor</u> through which signals sensed by the sensor can be read out to the pixel readout line, a first switch that can be enabled to read out signals from the sensor, and a reset switch;

a signal processing circuit that can be coupled to the pixel readout line; and

a controller configured to provide control signals to cause the pixel readout line to be clamped to a voltage level less than a voltage corresponding to a signal sensed by the sensor, and subsequently to cause the sensor signal to be read out through the ~~n-MOS~~ source-follower <u>transistor</u> to the pixel readout line and to be stored by the processing circuit,

<u>wherein the processing circuit includes a capacitive storage node, and wherein the controller is configured to provide control signals to cause the capacitive storage node to be clamped to a voltage less than a voltage corresponding to the sensor signal appearing on the pixel readout line, and subsequently to cause the pixel readout line to be coupled to the storage node.</u>

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17. (Withdrawn) The imager of claim 16 wherein the controller is configured to provide a control signal to cause the first switch to be disabled while a previously-stored sensor signal is being processed by the processing circuit.

18. (Currently Amended) The imager of claim 16, further comprising: including

a third switch coupled between the pixel readout line and ground,

wherein the controller is configured provide a control signal to cause the pixel readout line to be clamped by enabling the third switch.

19. (Canceled)

20. (Currently Amended) The imager of claim [[19]] 16, wherein the storage node is clamped to substantially the same voltage and at about the same time as the pixel readout line.

21. (Currently Amended) The imager of claim [[19]] 16, wherein:

the processing circuit further comprises includes a second capacitive storage node, and wherein

the controller is configured to provide control signals to cause the reset

switch in the pixel to be enabled, and subsequently to cause a reset signal to be

read out onto the pixel readout line through the ~~n-MOS~~ source-follower

<u>transistor</u>, and to cause a signal that corresponds to the reset signal to be stored

on the second capacitive storage node.

22-40. (Canceled)

41. (New) The method of claim 1, wherein the reading out the pixel signal onto

the pixel readout line comprises reading out the pixel signal through the source-

follower transistor.

42, (New) The method of claim 41, wherein the source-follower transistor

comprises an n-MOS transistor.

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